CLAIMS:

1. A measurement circuit comprising:

a plurality of measured elements; and

a plurality of sigma-delta modulators operating in a synchronized multi-phase cycle in which each sigma-delta modulator has an associated measurement phase, each sigma-delta modulator producing a digital output as a function of charge packets received from a different subset of the measured elements during its associated measurement phase, each different subset including one of the measured elements that is shared by the subsets.

2. The measurement circuit of claim 1 and further comprising:

a switching circuit having a plurality of switches for delivering charge packets as functions of the measured elements to the plurality of sigma-delta modulators; and

switch logic control for controlling the switching circuit as a function of the measurement phase and the digital output of the sigma-delta modulator associated with that measurement phase.

3. The measurement circuit of claim 2 wherein the switching circuit comprises:

input switches for selectively connecting the measured elements to positive and negative voltages;

charge packet delivery switches for selectively connecting the measured elements to the sigma-delta modulators; and

grounding switches for selectively connecting the measured elements to a ground potential.

4. The measurement circuit of claim 1 wherein the measured elements include capacitive sensor elements.

5. The measurement circuit of claim 4 wherein the measured element that is shared is a reference capacitor.

6. A measurement circuit comprising:

a first measured element;

a second measured element;

a third measured element;

a first charge packet integrating converter for producing first output as a function of a ratio of charge packets received;

a second charge packet integrating converter for producing a second output as a function of a ratio of charge packets received;

a drive signal source for providing drive signals to the first, second and third measured elements;

a switching circuit for selectively supplying charge packets from the first measured element and the third measured element to the first charge packet integrating converter and for selectively supplying charge packets from the second measured element and the third measured element to the second charge packet integrating converter; and

switch control logic for controlling the switching circuit so that the first charge packet integrating converter receives charge packets during a first phase and the second charge packet

integrating converter receives charge packets during a second phase.

7. The measurement circuit of claim 6 wherein the switch control logic controls the switching circuit as a function of the first output during the first phase and as a function of the second output during the second phase.

8. The measurement circuit of claim 6 wherein the switching circuit comprises:

charge packet delivery switches for controlling delivery of charge packets to the converters; and

grounding switches for selectively connecting the first, second and third measured elements to a ground potential.

9. The measurement circuit of claim 6 wherein the first and second measured elements are capacitive sensor elements.

10. The measurement circuit of claim 6 wherein the first and second measured elements are absolute pressure sensors.

11. The measurement circuit of claim 6 wherein the third measured element is a capacitor.

12. The measurement circuit of claim 6 and further comprising:

a digital signal processor for producing a plurality of digital outputs as a function of the first and second outputs.

13. The measurement circuit of claim 6 wherein the first and second

charge packet integrating converters comprise sigma-delta modulators.

14. The measurement circuit of claim 13 wherein the sigma-delta modulators are second order sigma-delta modulators.

15. The measurement circuit of claim 6 wherein the third measured element has a fixed value.

16. The measurement circuit of claim 6 wherein the third measured element has a variable value.

17. A measurement circuit comprising:

a plurality of sensor elements;

a shared element; and

a plurality of sigma-delta modulators operating in a synchronized multi-phase cycle in which each sigma-delta modulator has an associated measurement phase, each sigma-delta modulator producing a digital output as a function of charge packets received from at least one of the sensor elements and the shared element during its associated measurement phase.

18. The measurement circuit 17 and further comprising:

a switch circuit having a plurality of switches for delivering charge packets as functions of the sensor elements and the shared element to the plurality of sigma-delta modulators; and

switch logic control for controlling the switching circuit as a function of the measurement phase and the digital output of

the sigma-delta modulator associated with that measurement phase.

19. The measurement circuit of claim 18 wherein the switching circuit comprises:

input switches for selectively connecting the sensor elements and the reference element to positive and negative voltages;

charge packet delivery switches for selectively connecting the sensor elements and the shared element to the sigma-delta modulators; and

grounding switches for selectively connecting the sensor elements and the reference element to a ground potential.

20. The measurement circuit of claim 17 wherein the sensor elements are capacitive sensor elements.

21. The measurement circuit of claim 20 wherein the shared element is a reference capacitor.

22. The measurement circuit of claim 17 wherein the shared element is a sensor having a variable value.

23. The measurement circuit of claim 17 wherein the shared element is a reference element having a fixed value.

24. A measurement circuit comprising:

a first sensor element;

a second sensor element;

a first charge packet integrating converter for producing first output as a function of a rate of packets received;

a second charge packet integrating converter for producing a second output as a function of a ratio of packets received;

a shared element;

a drive signal source for providing drive signals to the first and second sensor elements and the shared element;

a switching circuit for selectively supplying charge packets from the first sensor element and the shared element to the first charge packet integrating converter and for selectively supplying charge packets from the second sensor element and the shared element to the second charge packet integrating converter; and

switch control logic for controlling the switching circuit so that the first charge packet integrating converter receives charge packets during a first phase and the second charge packet integrating converter receives charge packets during a second phase.

25. The measurement circuit of claim 24 wherein the switch control logic controls the switching circuit as a function of the first output during the first phase and as a function of the second output during the second phase.

26. The measurement circuit of claim 24 wherein the switching circuit comprises:

charge packet delivery switches for controlling delivery of packets to the converters; and

grounding switches for selectively connecting the first and second sensor elements and the shared element to a ground potential.

27. The measurement circuit of claim 24 wherein the first and second sensor elements are capacitive sensor elements.

28. The measurement of claim 24 wherein the first and second sensor elements are absolute pressure sensors.

29. The measurement circuit of claim 24 wherein the shared element is a capacitor.

30. The measurement circuit of claim 24 and further comprising:

a digital signal processor for producing a plurality of digital outputs as a function of the first and second outputs.

31. The measurement circuit of claim 24 wherein the first and second charge packet integrating converters comprise sigma-delta modulators.

32. The measurement circuit of claim 31 wherein the sigma-delta modulators are second order sigma-delta modulators.

33. The measurement circuit of claim 24 wherein the shared element has fixed value.

34. The measurement circuit of claim 24 wherein the shared element has a variable value.